claims 1-56 are now pending in the present application and, for the reasons set forth in detail below, are believed to be in condition for allowance.

One feature of the present invention is the provision of an organic resin film to provide a leveled upper surface over a substrate having at least a thin film transistor thereon, and a liquid crystal material having ferroelectricity or anti-ferroelectricity. In accordance with the present invention, it is advantageous to employ a leveling film in a liquid crystal display (LCD) with a ferroelectric liquid crystal (FLC) material or an anti-ferroelectric liquid crystal (AFLC) material. When FLC or AFLC material is used in a LCD, a distance (called a cell gap) between two substrates having the liquid crystal material interposed therebetween should be shorter than when a nematic liquid crystal material is used. A cell gap for FLC or AFLC LCD is in a range of 1-2μm, typically, 1.5μm. On the other hand, a cell gap of a nematic LCD is usually in a range of 4-5 μm.

When the cell gap is narrow, the surface flatness of each of the two substrates is important with respect to the display properties of the LCD. If the surfaces are rough, light does not pass evenly through the substrate, so that a display having good performance characteristics cannot be realized.

Because a plurality of thin film transistors are formed over one of the substrates (a TFT substrate), the surface of the TFT substrate is very rough (i.e. uneven). In addition, the other one of the substrates (an opposite substrate) has other elements of the LCD formed thereover, for example, a color filter. Therefore, it is advantageous to form the leveling film over not only the TFT substrate but also the opposite substrate in order to flatten each of the upper surfaces of the two substrates.

Also, variation in cell gaps of LCDs using FLC or AFLC material is more detrimental to the performance characteristics than variations in LCDS using a nematic liquid crystal material. Accordingly, it is more preferably to employ a leveling film in LCDs using FLC or AFLC materials.

Referring now to the Official Action, it is first noted that the references listed on the 1449 forms filed in this application are not available to the Examiner in the related

applications and copies are requested from applicant. In response, applicant is currently obtaining copies of the cited references and will submit them for consideration by the Examiner as soon as possible. The Examiner's attention is also directed to three copending applications, as noted under separate cover submitted herewith.

Paragraph 1 of the Official Action objects to the title of the application as not being descriptive. In response, the title has been amended herewith and reconsideration is requested in view thereof.

Paragraph 2 of the Official Action rejects claims 1-4, 9-16, 21-28, 33-34 and 45-48 as obvious based on the combination of U.S. Patent 5,227,900 to Inaba et al. and JP 61-141174. Initially, applicant notes that the Official Action refers to Japanese Patent Laid-Open No. 61-141174 as "Yamato," apparently indicating "Yamato" as an inventor as is conventional. However, "Yamato" is not the inventor's name but rather a part of the address of the inventors. Attached is a copy of a full translation of JP 61-141174, which is believed to be of record in the present application, indicating the inventors as Takeshita, Kurihara, Oka and Hasegawa. To avoid confusion, this response refers to the '174 reference alternatively as Yamato and Takeshita et al.

Substantively, applicant notes that Inaba '900 does not teach the feature of a leveling film in accordance with the present invention but rather is relied upon for teaching the use of FLC, while Yamato (Takeshita et al.) is relied upon for teaching the leveling film. The Official Action asserts that it would have been obvious to combine the teachings of Inaba and Yamato (Takeshita et al.).

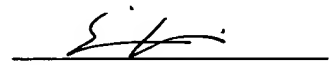
Applicant notes that the burden of establishing a *prima facie* case of obviousness under §103 lies with the Patent Office. In re Fine, 5 USPQ2d 1596 (Fed. Cir. 1988). To establish a *prima facie* case of obviousness, there must be (1) some suggestion or motivation (either in the references themselves or in the knowledge generally available to one of ordinary skill in the art) to modify the reference or to combine reference teachings to achieve the claimed invention and (2) the prior art must teach or suggest all the claim limitations. MPEP §2143.

In the present application, however, the claimed invention includes the recitation of a leveling film used to cover a surface of a TFT substrate of a LCD including at least one of FLC or AFLC materials. It is respectfully submitted that it is not possible to realize the present invention by only applying Inaba to Yamato (Takeshita et al.). That is, it is respectfully submitted that the combination of Inaba and Yamato (Takeshita et al.) would not teach or suggest all of the claim limitation as required to maintain a *prima facie* case of obviousness.

Furthermore, it is respectfully submitted that the Official Action has failed to establish sufficient motivation for one of skill in the art to combine the references. That is, simply because the references could be combined, does not mean they should be. MPEP §2143.01, citing In re Mills, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990). In the Official Action, it is respectfully submitted that there has been an insufficient showing that one of skill in the art would have been led to combine and/or modify the references relied upon in a manner to achieve the present invention and reconsideration is requested for this further reason.

For all of the above reasons, Applicant believes that claims 1-56 are now in proper condition for allowance and reconsideration of the pending rejections and examination of the newly submitted claims is requested. If the Examiner feels that any further discussions would advance the prosecution of this case, it is respectfully requested that the undersigned be contacted.

Respectfully submitted,



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1. Title of the Invention: Solid state image pickup device
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SPECIFICATION

1. Title of the Invention

Solid state image pickup device

2. Scope of Claim for Patent

1. A solid state image pickup device of a type of detecting an amount of stored/discharged charges by a light receptive element formed on an insulating substrate, characterized in that a capacitor is provided with an upper electrode in parallel with said light receptive element by oxidizing a portion of a lower electrode of the light receptive element.

2. The solid state image pickup device according to claim 1 characterized in that an amorphous silicon is used as the light receptive element, chromium or aluminum is used as the lower electrode and an additional capacitance of an oxide film is formed simultaneously with phothoetching the amorphous silicon film.

3. Detailed Description of the Invention

"Field of the Invention in Industry"

The present invention relates to a solid state image pickup device utilizing solid state image pickup elements.

"Prior art"

Conventionally, CCD type or MOS type is practicable as a solid state image pickup element. In compared with an image pickup tube, the solid state image pickup element is proof against vibration and clash. The solid state image pickup element is characterized in very little power consumption to be used for a long span. Further, MOS type has bigger numerical aperture and has no limit of the amount of transfer charge compared to CCD type, so that a lot of signal can be output. However, MOS type has a defect of occurring a great noise. Fig. 3 shows a drawing of typical MOS type circuit. Referring to the drawing, the cause of noise occurrence will be described. The noise is caused by horizontal MOS FET switch which opens or closes a circuit. It is most serious problem, which causes in the case that a wiring capacitance on vertical lines V_1 to V_n is large and electrode- substrate capacitance of transistors formed on V_1 to V_n is large, so that noise charge which remains on the lines is read out. There is no comparison between the amount of noise and the capacitance of

the receptive portion, so that the S/N ratio is considerably decreased. In addition to the above mentioned problem of noise, there is one more problem of smear for both CCD type and MOS type. One of reasons is due to occurrence charge caused by light, which is incident upon the other portion in addition to the receptive portion, is signal lines.

Therefore, elements in thin film form is formed by utilizing an insulator as a substrate, so that wiring capacitance is considerably reduced. Further, S/N ratio is increased by forming additional capacitor on the receptive element. For example, as the additional capacitor, a thin film such as SiO_2 or Y_2O_3 is deposited in addition.

"Problem To Be Solved by The Invention"

However, in the above mentioned prior art, an additional thin film has to be formed in order to connect a receptive element with an additional capacitor. Therefore, process steps will increase to cause cost up. As a result, noise will be caused because a thin film will not be formed uniformly.

Therefore, the present invention will solve the problem. An object of the present invention is to provide a solid state image pickup device having an additional capacitor with high evenness in parallel with the receptive element without increasing the process steps.

"Means To Solve The Problem"

The solid state image pickup device in the present invention is characterized in that the additional capacitor with high evenness can be easily formed in parallel with the receptive element by a method wherein a part of lower electrode of receptive element is oxidized by utilizing receptive element portion as a mask to provide a capacitor between upper and lower electrodes.

In particular, the present invention is utilized an oxidation film formed by a method wherein receptive element is performed photoetching by the technique of dry etching using Freon gas comprising oxygen. Moreover, the present invention utilizes an amorphous silicon for the portion of receptive element and a polycrystalline silicon for the drive portion, respectively. Through these procedures, the solid state image pickup device having small amount of smear can be formed increasing sensitivity and saturated light quantity.

"Performance"

According to the above mentioned structure in the present invention, an oxidation film formed on lower electrode of a receptive element will be

an additional capacitor between lower electrode and upper electrode. As a result, the solid state image pickup element having small noise will be formed increasing saturated light quantity and S/N ratio.

"Example"

Fig. 1 shows a configuration drawing in accordance with the present example of the present invention. Any receptive element or switching element can be used for a semiconductor substrate. In the present invention, an amorphous silicon photodiode is used as a receptive element, and poly-silicon TFT is used as a switching element, respectively. Fig. 2 shows an equivalent circuit of Fig. 1. In Fig. 1, (a) shows a cross sectional view and (b) shows a plan view. Process steps will be described as follows. A non-doped polycrystalline silicon layer 102 is formed on an insulating substrate 101 such as quartz glass and after forming a gate insulating film by thermal oxidation, a second polycrystalline silicon 103 to be a gate electrode is formed to be also a gate line. Subsequently, ion is implanted to provide a source and drain electrode. Then, after forming SiO_2 or the like as an interlayer insulating film 104, a contact hole is formed and a vertical line 105 is formed with a conductive material such as Al, upon which a polyimide resin or the like 106 is formed for leveling as an interlayer insulating film. Usually, poly-silicon TFTs are formed by the above mentioned method. Significant process steps according to the present invention will be described as follows. After forming a contact hole on the interlayer insulating film, a conductive thin film 107 is formed by using such as Cr or Al as lower electrode of pixel. This conductive thin film 107 should be easily oxidized and the oxide film should be high resistivity and dense since it is oxidized after the formation of the receptive film 108 using the receptive film(a photo resist may be disposed thereon) as a mask in order to form an additional capacitor. As an oxidation method, it can be considered various kinds of method, however, in case that a receptive film 108 is etched by plasma using oxygen and Freon, an oxidation film 109 is formed as a necessary result, so that there is no need to add oxidation process. After oxidation by the method, oxide plasma treatment may be further conducted, or oxidation with thermal nitric acid or steam oxidation may be conducted. Table 1 shows a characteristic example of forming a lower electrode 107 by using oxidation of Cr and Al-Si and in accordance with the present example. Here, the receptive film thin 108 is an amorphous silicon (referred to a-Si, hereinafter) formed by GD plasma CVD,

and 110 may be any transparent conductive electrode (upper electrode), here, ITO.

Table 1

CONDITION	ELEMENT CAPACITY ($pF/100\mu m^2$)	INSULATION PROPERTY
(1) a-Si is etched by using $CF_4 + O_2$	0.2	good
(2) O_2 plasma treatment in addition to (1)	0.5	best
(3) thermal nitrate treatment in addition to (1)	0.5	good
(4) using Al-Si as electrode with condition (2)	0.2	regular
(5) oxidation by steam using Al-Si as electrode	0.3	good

Note) An electrode used in conditions (1) to (3) is Cr.

In the table 1, an amount of the element capacity is calculated by adding capacitance of a-Si to additional capacitor of an oxidation film. The capacitance of a-Si is approximately $0.01pF/100\mu m^2$. Regarding to the uniformity, the condition (3) is best of all. Under the condition (3), dispersion of all elements is within a range of $\pm 1\%$, and under the other conditions, it is within a range of $\pm 2.5\%$. In any way, it is easier than the case of forming SiO_2 or dielectric thin film in additional process and probability of dispersion is small. (in case of SiO_2, the dispersion is within a range of $\pm 5\%$)

Referring to the equivalent circuit in Fig. 2, through the above mentioned process, the circuit is provided with an additional capacitor Ca in parallel with the receptive element Dil.

Moreover, metal is used as a lower electrode in the above mentioned example. Instead of using the metal, by using low resistance amorphous silicon which is doped impurities, an oxidation may be performed to form SiO_2 in order to use the SiO_2 as an additional capacitor.

"The effect of the Invention"

As mentioned above, according to the present invention, since the additional capacitor having a high uniformity can be formed extremely

easily and inexpensively without increasing the process steps by using the pattern of a thin film receptive element as a mask, it is possible to easily obtain excellent solid image pickup devices with low cost having a large S/N ratio and a large saturated light quantity.

4. Brief Explanation of The Drawings

Fig. 1 is example of a solid state image pickup device in the present invention wherein (a) is a cross sectional view and (b) is a plan view.

Fig. 2 is a equivalent circuit drawing of the example.

Fig. 3 is a usual circuit drawing of MOS type solid state image pickup device.

101---substrate
103---gate electrode
105---vertical line
107---lower electrode
108---receptive thin film
109---oxidation film
110---upper electrode

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